

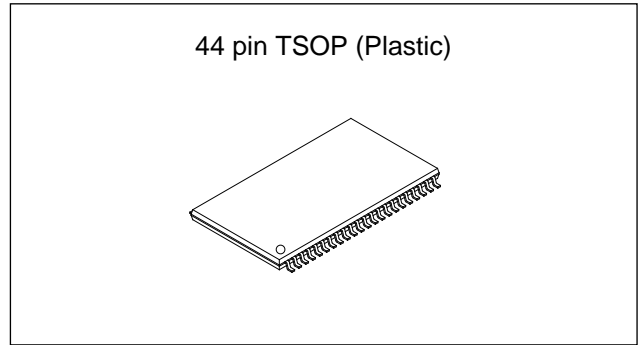
65536-word × 18-bit High Speed Bi-CMOS Static RAM

Description

CXK5B18120TM is a high speed 1M bit Bi-CMOS static RAM organized as 65536 words by 18 bits. Operating on a single 3.3V supply this asynchronous IC is suitable for use in high speed and low power applications.

Features

- Single 3.3V Supply 3.3V±0.3V
- Fast access time 12ns (Max.)
- Low stand-by current: 10mA (Max.)
- Low power operation 1116mW (Max.)
- Package line-up
Dual Vcc/Vss
CXK5B18120TM 400mil 44pin TSOP Package



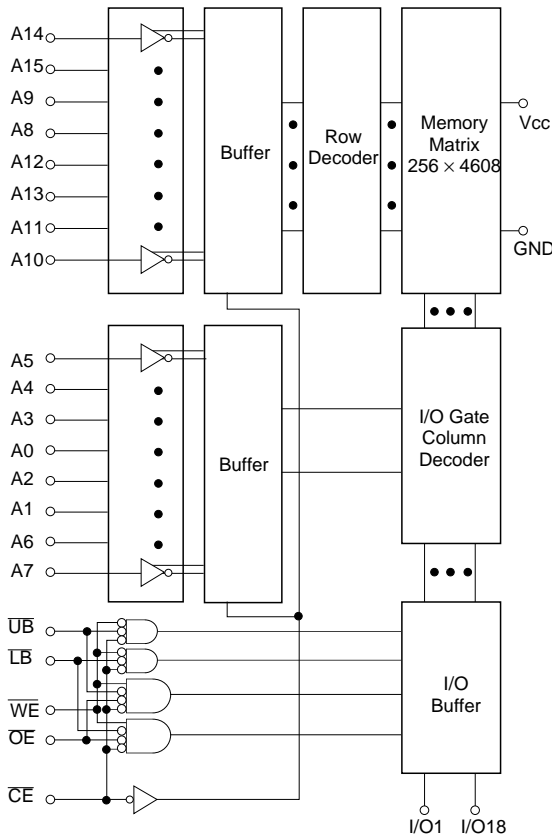
Function

65536-word × 18-bit static RAM

Structure

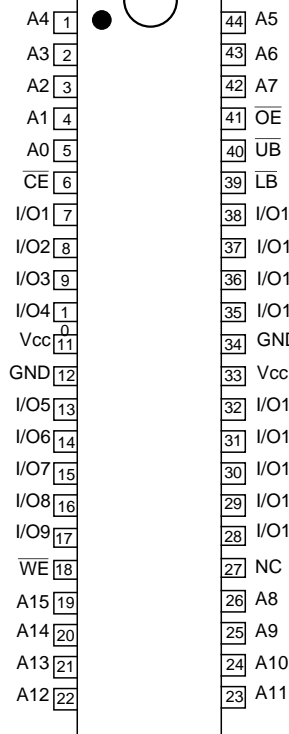
Silicon gate Bi-CMOS IC

Block Diagram



Pin configuration

(Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O9	Data input output (lower byte I/O)
I/O10 to I/O18	Data input output (upper byte I/O)
CE	Chip enable input
WE	Write enable input
OE	Output enable input
LB	Lower byte select input
UB	Upper byte select input
Vcc	+3.3V Power supply
GND	Ground
NC	No connection

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Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* ¹ to +4.6	V
Input voltage	V _{IN}	-0.5* ¹ to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* ¹ to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.5* ²	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

*1 V_{CC}, V_{IN}, V_{I/O} = -2.0V Min. for pulse width less than 5ns

*2 Air Flow ≥ 1m/s

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	Mode	I/O1 to I/O9	I/O10 to I/O18	Current
H	×	×	×	×	Not selected	High Z	High Z	I _{SB1} , I _{SB2}
L	L	H	L	L	Read	Data Out	Data out	I _{CC}
			L	H	Read	Data Out	High Z	I _{CC}
			H	L	Read	High Z	Data out	I _{CC}
			H	H	Not selected	High Z	High Z	I _{CC}
L	×	L	L	L	Write	Data in	Data in	I _{CC}
			L	H	Write	Data in	High Z	I _{CC}
			H	L	Write	High Z	Data in	I _{CC}
L	H	H	×	×	Output disable	High Z	High Z	I _{CC}
L	×	×	H	H	Not selected	High Z	High Z	I _{CC}

×: "H" or "L"

Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.0	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -2.0V Min. for pulse width less than 5ns

Electrical Characteristics

DC Characteristics

(V_{CC} = 3.3V±0.3V, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-10	—	+10	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ V _{I/O} = GND to V _{CC}	-10	—	+10	μA
Average operating current	I _{CC}	Min. Cycle Duty = 100% I _{OUT} = 0mA, $\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL}	—	—	310	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	10	mA
	I _{SB2}	Min. Cycle Duty = 100% $\overline{CE} = V_{IH}$, V _{IN} = V _{IH} or V _{IL}	—	—	100	mA
Output high voltage	V _{OH}	I _{OH} = -2.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.0mA	—	—	0.4	V

* V_{CC} = 3.3V, Ta = 25°C

I/O Capacitance

(Ta = 25°C, f = 1MHz)

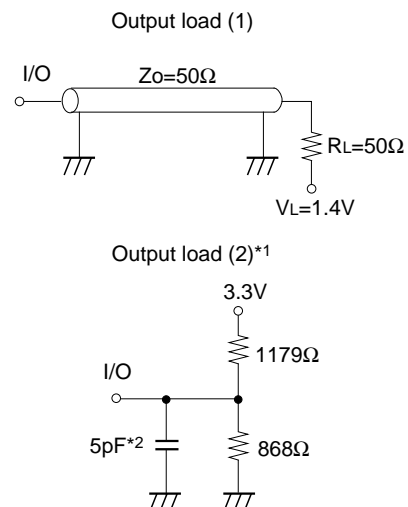
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	5	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test condition** (V_{CC} = 3.3V±0.3V, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0.0V
Input rise time	t _r = 2ns
Input fall time	t _f = 2ns
Input and output reference level	1.4V
Output load conditions	Fig. 1



*1. For t_{LZ}, t_{OLZ}, t_{LBLZ}, t_{UBLZ}, t_{HZ}, t_{OHZ}, t_{LHZ}, t_{UBHZ}, t_{OW}, t_{WHZ}

*2. Including scope and jig capacitances.

Fig. 1

• Read cycle

Item	Symbol	-12		Unit
		Min.	Max.	
Read cycle time	t_{RC}	12	—	ns
Address access time	t_{AA}	—	12	ns
Chip enable access time	t_{CO}	—	12	ns
Output enable to output valid	t_{OE}	—	6	ns
Byte select to output valid	t_{LB}, t_{UB}	—	6	ns
Output data hold time	t_{OH}	3	—	ns
Chip enable to output in low Z (\overline{CE})	t_{LZ}^*	3	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}^*	0	—	ns
Byte select to output in low Z ($\overline{LB}, \overline{UB}$)	t_{LBLZ}, t_{UBLZ}^*	0	—	ns
Chip disable to output in high Z (\overline{CE})	t_{HZ}^*	0	6	ns
Output disable to output in high Z (\overline{OE})	t_{OHZ}^*	0	6	ns
Byte select to output in high Z ($\overline{LB}, \overline{UB}$)	t_{LBHZ}, t_{UBHZ}^*	0	6	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

This parameter is sampled and is not 100% tested.

• Write cycle

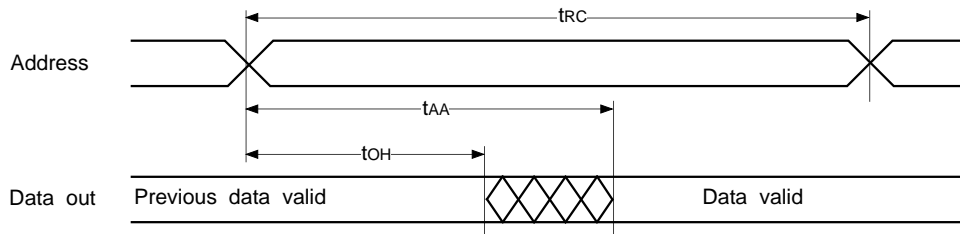
Item	Symbol	-12		Unit
		Min.	Max.	
Write cycle time	t_{WC}	12	—	ns
Address valid to end of write	t_{AW}	10	—	ns
Chip enable to end of write	t_{CW}	10	—	ns
Byte select to end of write	t_{LBW}, t_{UBW}	10	—	ns
Data valid to end to write	t_{DW}	8	—	ns
Data hold from end of write	t_{DH}	0	—	ns
Write pulse width	t_{WP}	10	—	ns
Address set up time	t_{AS}	0	—	ns
Write recovery time	t_{WR}	0	—	ns
Output active from end of write	t_{OW}^*	4	—	ns
Write to output in high Z	t_{WHZ}^*	0	6	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

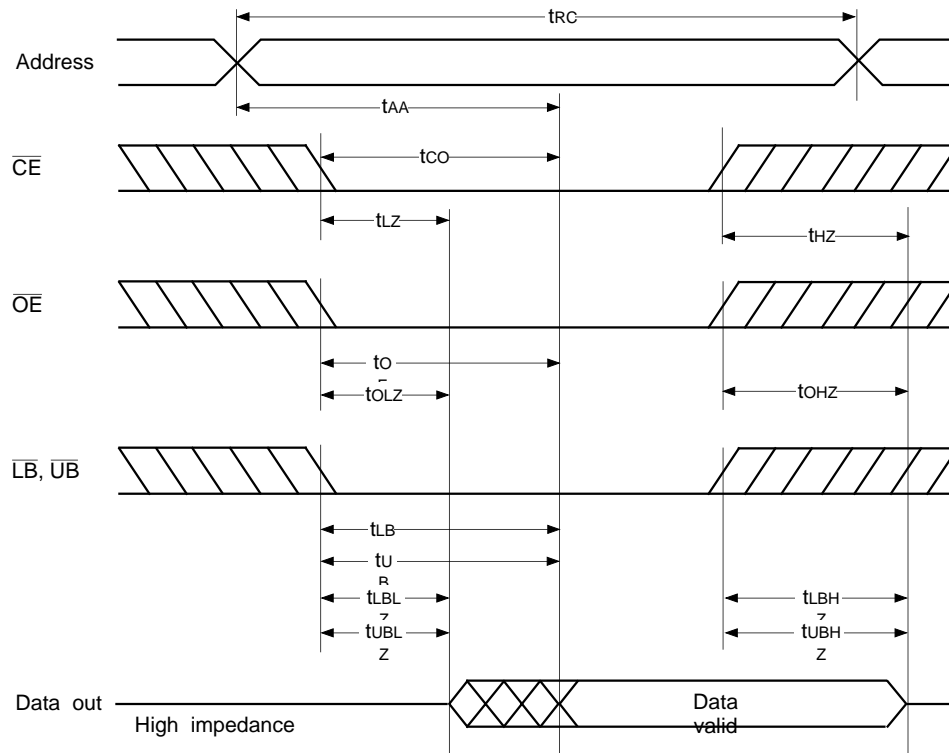
This parameter is sampled and is not 100% tested.

Timing Waveform

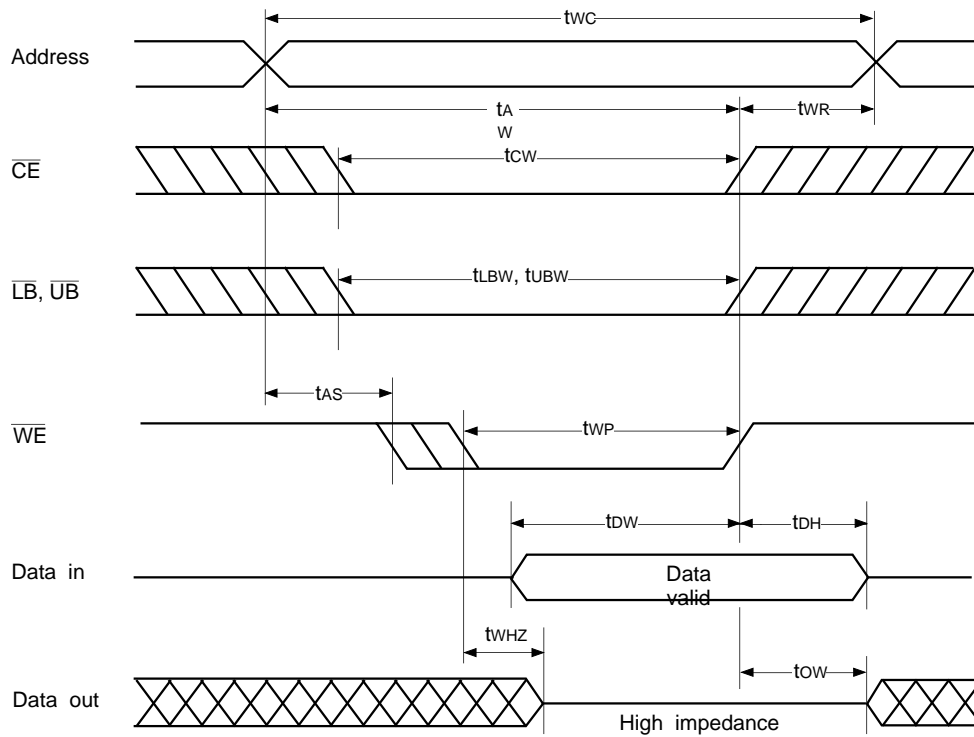
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



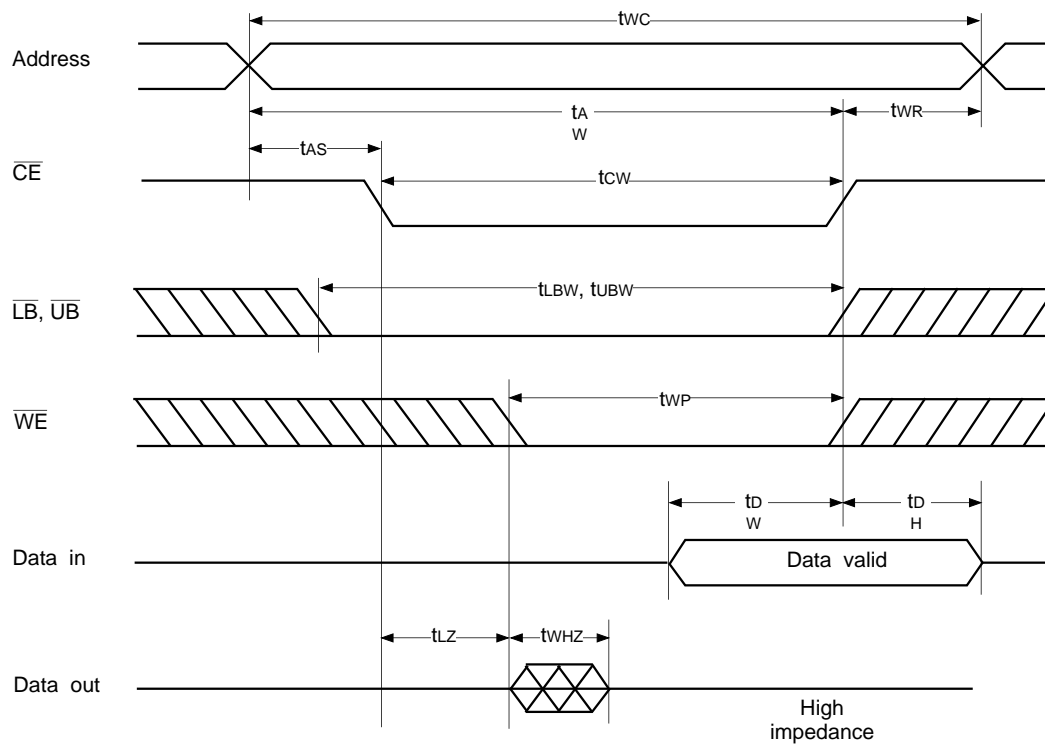
- Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : WE control

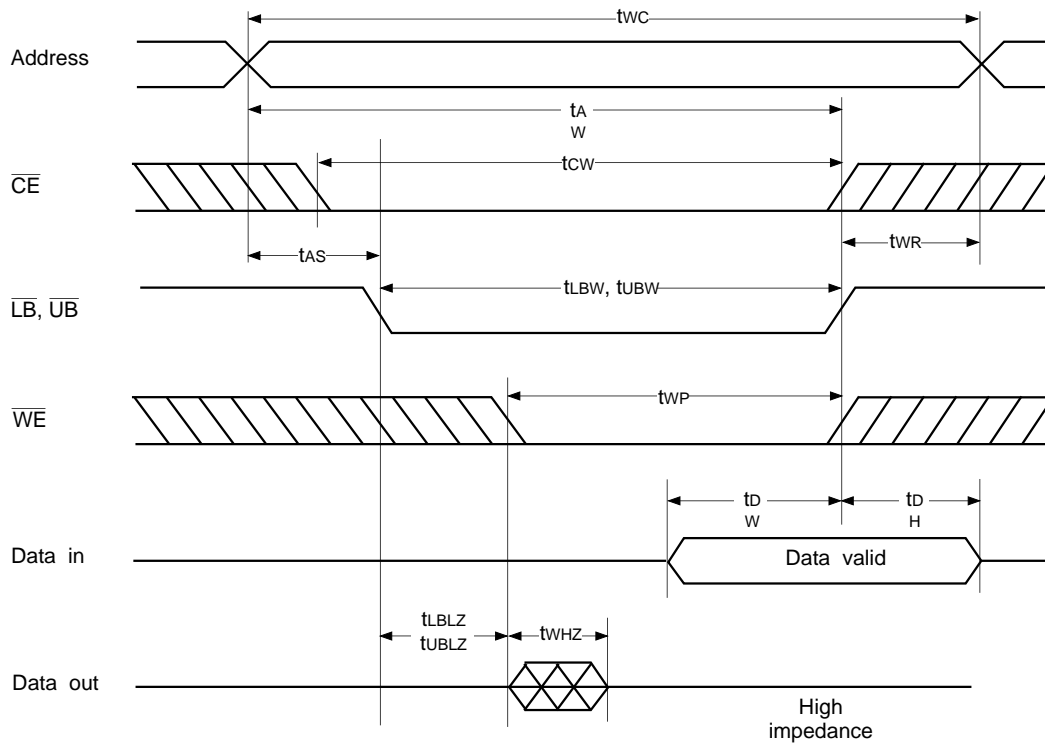


• Write cycle (2) : \overline{CE} control



* Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

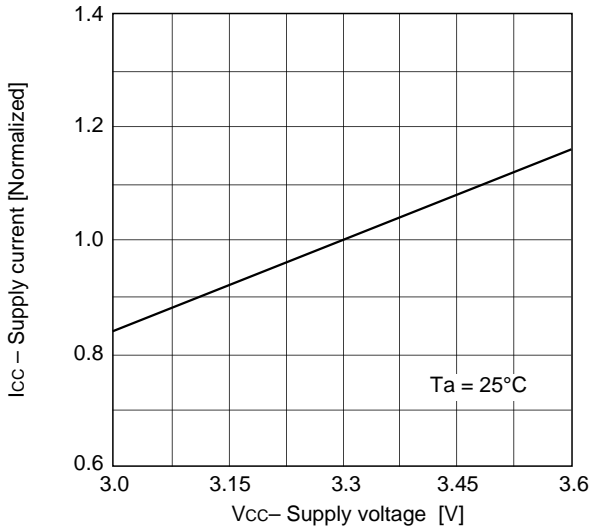
• Write cycle (3) : LB, UB control



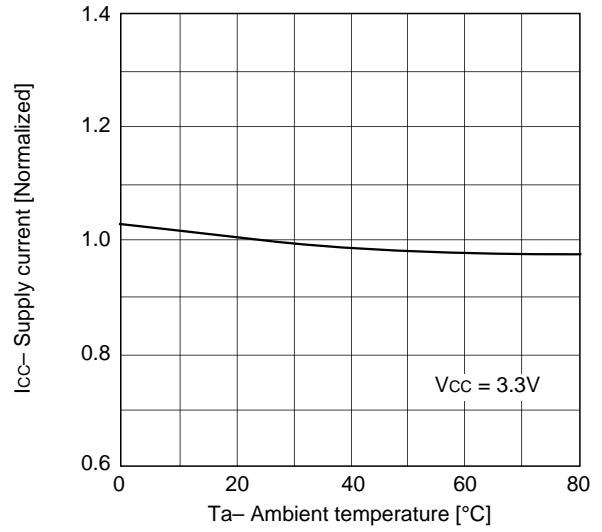
* Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Example of Representative Characteristics

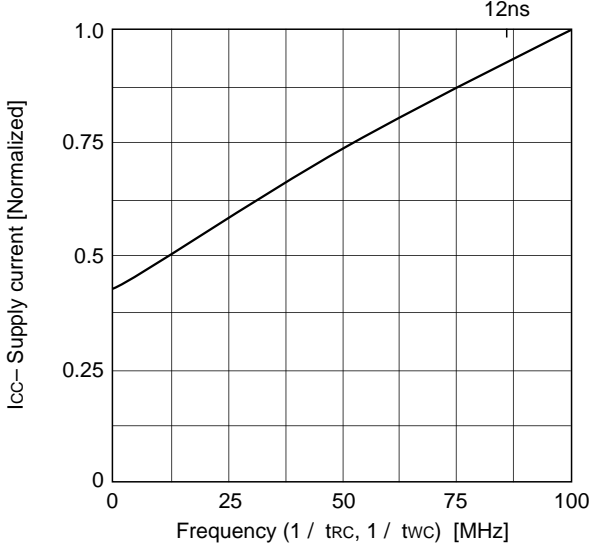
Supply current vs. Supply voltage



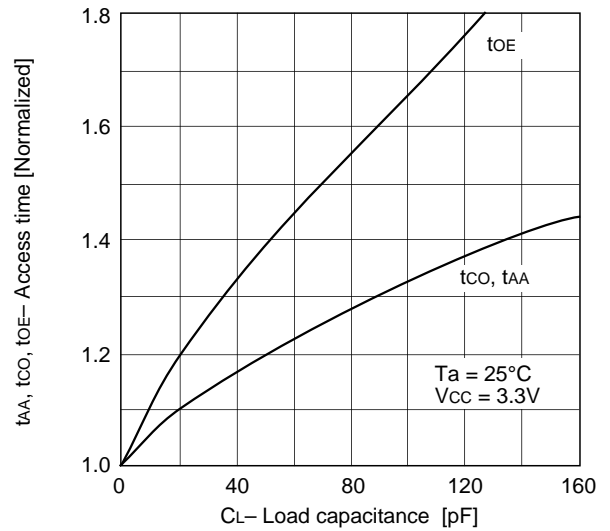
Supply current vs. Ambient temperature



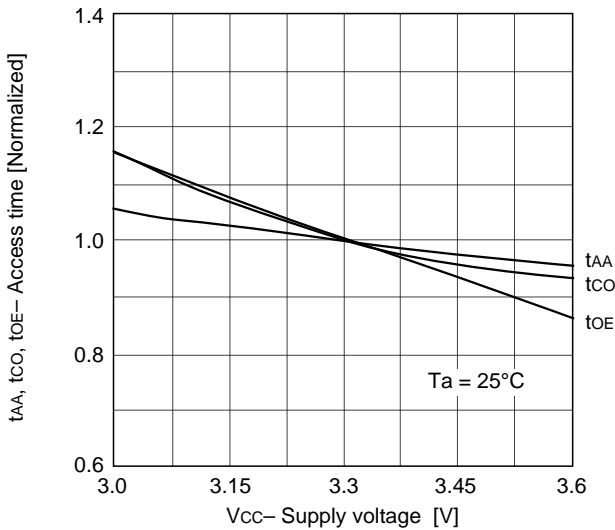
Supply current vs. Frequency



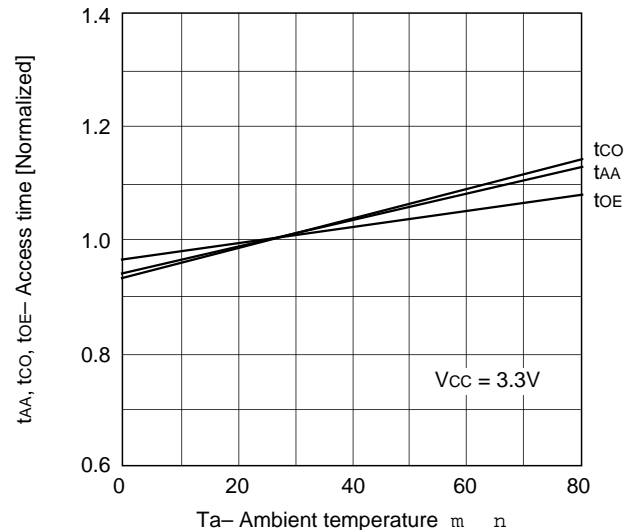
Access time vs. Load capacitance



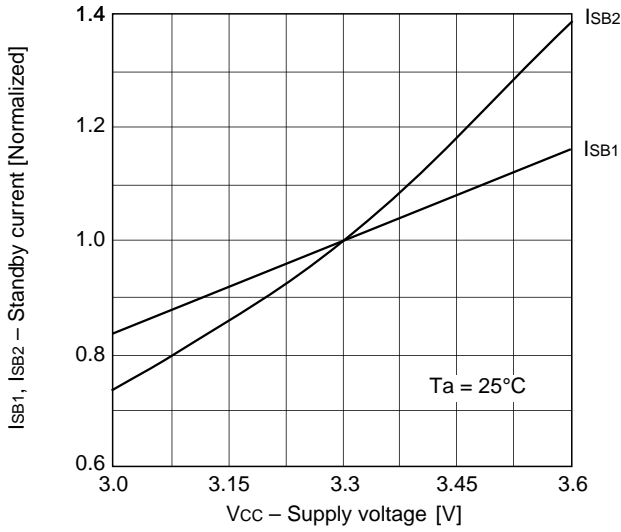
Access time vs. Supply voltage



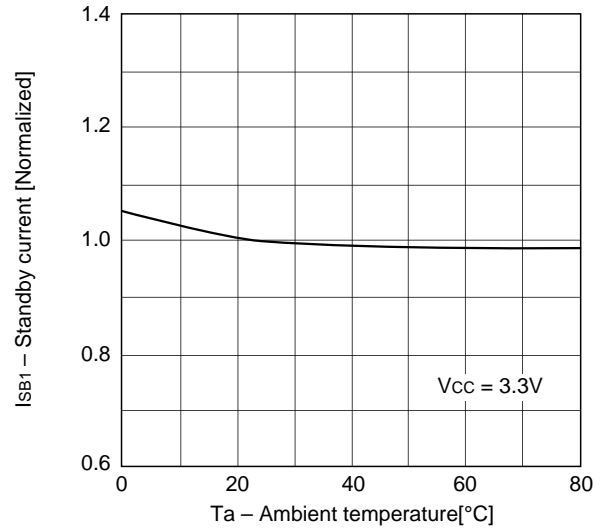
Access time vs. Ambient temperature



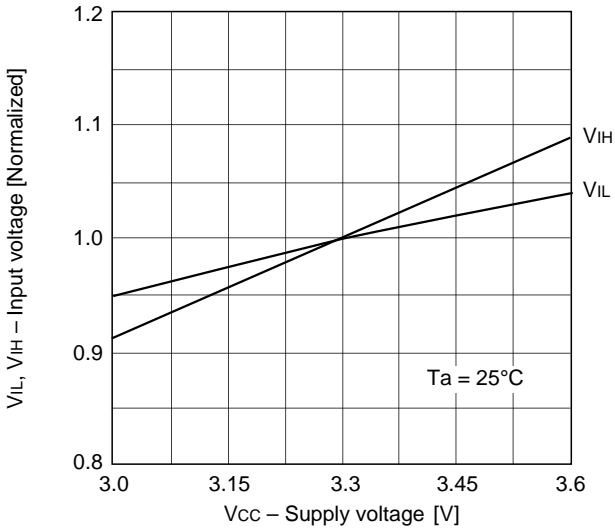
Standby current vs. Supply voltage



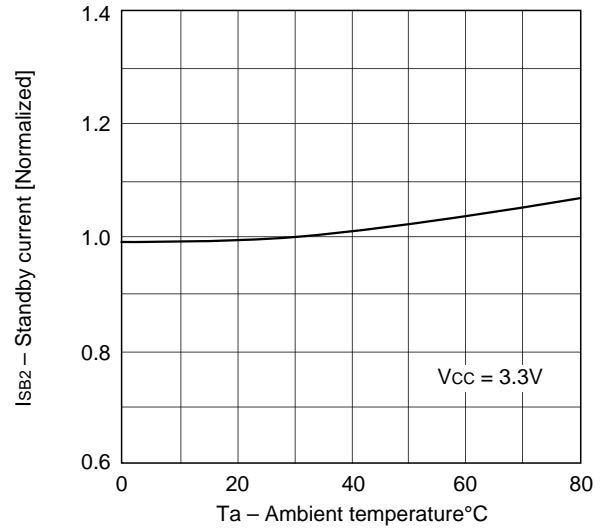
Standby current vs. Ambient temperature



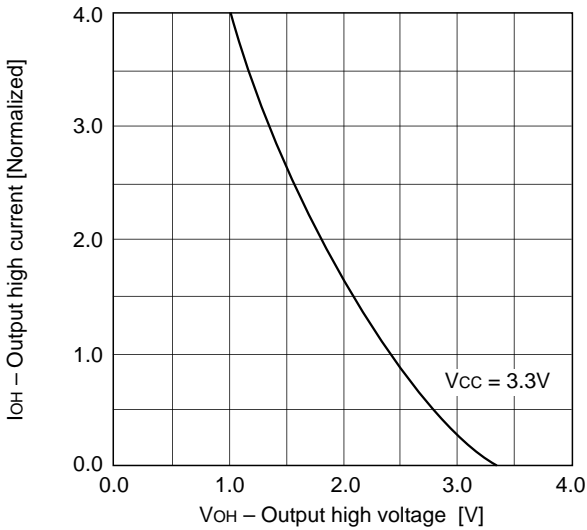
Input voltage level vs. Supply voltage



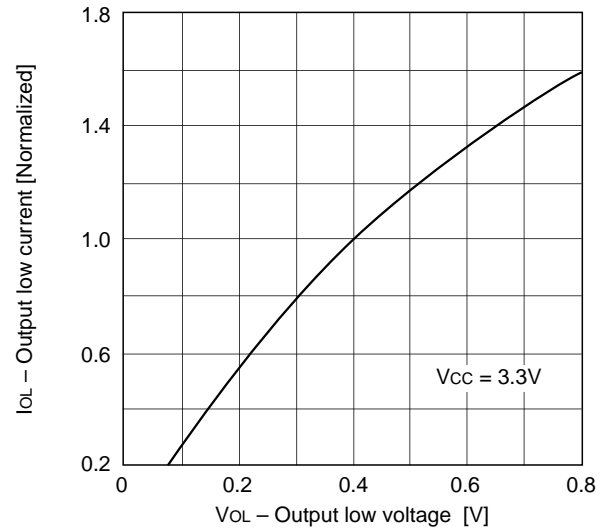
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

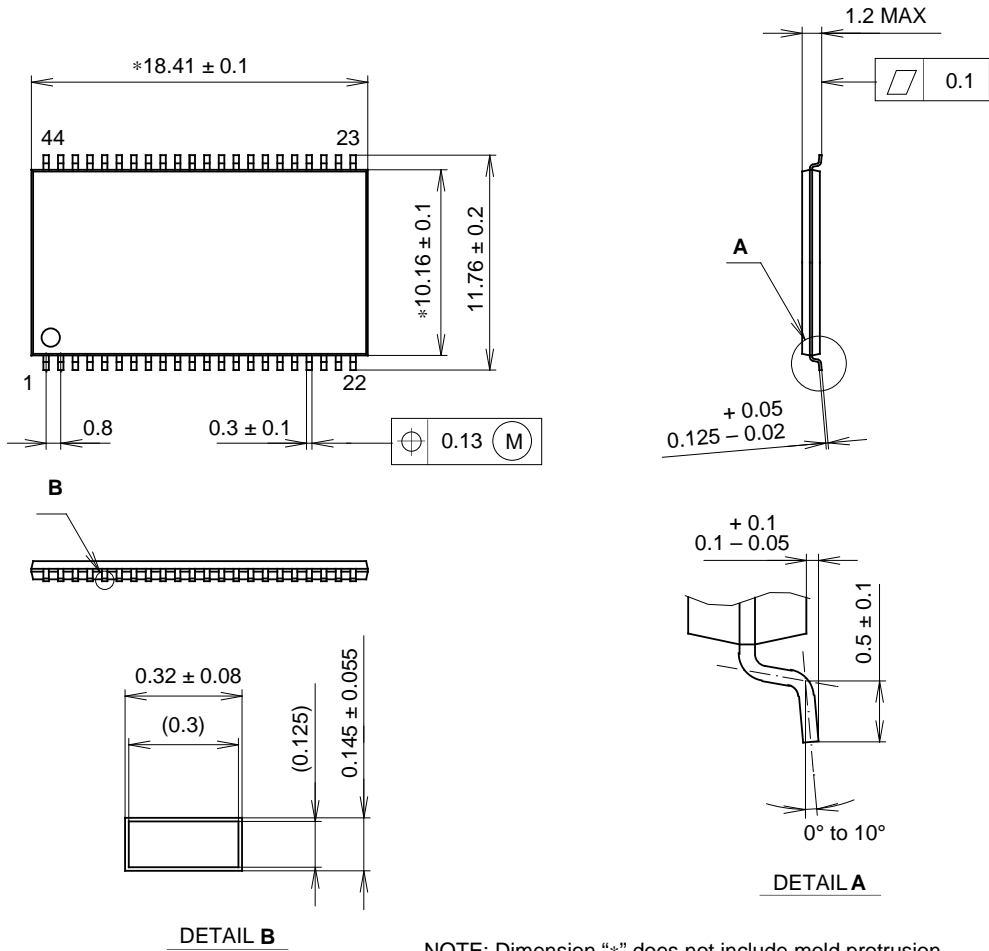


Output low current vs. Output low voltage



Package Outline Unit: mm

44PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01
EIAJ CODE	TSOP (II) 044-P-0400-A
JEDEC CODE	—

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g